IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A method for wear leveling of a multi-block memory ~~(10)~~ containing data, usable in multi-block memory ~~(10)~~ activities, comprising ~~the steps of~~:

detecting ~~(42, 42a)~~ an at least one triggering signal ~~(26)~~; and

copying or relocating ~~(52, 52a)~~ the data of an at least one first memory block ~~(17)~~ containing an at least one memory element of the multi-block memory ~~(10)~~ to an at least one second memory block ~~(18)~~ of the multi-block memory ~~(10)~~ after detecting ~~(42, 42a)~~ the at least one triggering signal, wherein said at least one second memory block ~~(18)~~ does not contain said data before said copying or relocating,

wherein no information on a usage of said at least one first memory block, at least one second memory block or at least one memory element is provided for performing said copying or relocating.

2. (Currently Amended) The method according to claim 1, wherein each of the at least one first memory block ~~(17)~~ and the at least one second memory block ~~(18)~~ contains only one memory element.

3. (Currently Amended) The method according to claim 1, further comprising the step of:

updating ~~(54)~~ a first memory pointer M ~~(M)~~ originally pointed to the at least one second memory block ~~(18)~~ before

said copying or relocating to point to the at least one first memory block ~~(17)~~ after said copying or relocating.

4. (Currently Amended) The method according to claim 3, further comprising the step of:

updating ~~(58)~~ a second memory pointer Z ~~(Z)~~ by shifting it back to a physical zero point Z_0 ~~(Z_0)~~ by reducing the value of the second memory pointer Z ~~(Z)~~ by a number of relocated memory elements of the second memory block ~~(18)~~ if the first memory pointer M ~~(M)~~ is pointing to one of the memory elements of the at least one second memory block ~~(18)~~ after said updating.

5. (Currently Amended) The method according to claim 1, wherein there is more than one memory element contained in the at least one first memory block ~~(17)~~ and there is more than one memory element contained in the at least one second memory block ~~(18)~~, respectively.

6. (Currently Amended) The method according to claim 1, wherein the data of an at least one additional block of the multi-block memory ~~(10)~~ is relocated to an at least one further additional block of the multi-block memory ~~(10)~~ after detecting ~~(42, 42a)~~ the at least one triggering signal, wherein said at least one further additional block does not contain the data before said relocation.

7. (Original) The method according to claim 1, wherein said copying or relocating is performed according to predetermined criteria.

8. (Currently Amended) The method according to claim 7, wherein said predetermined criteria enables said copying or relocating of a regular pattern such that after a predetermined number of triggering signals ~~(26)~~, said copying or relocating ~~steps are~~ is identical to the copying or relocating performed in response to said predetermined number of the triggering signals.

9. (Currently Amended) The method according to claim 7, wherein said predetermined criteria enables said copying or relocating of a random pattern such that after any number of triggering signals ~~(26)~~, said copying or relocating ~~steps are~~ is not ~~necessarily~~ identical to the copying or relocating performed in response to said any number of the triggering signals.

10. (Currently Amended) The method according to claim 1, wherein said copying or relocating ~~(52, 52a)~~ of the data occurs only after detecting a predetermined number of the at least one triggering signal ~~(26)~~.

11. (Currently Amended) The method according to claim 1, wherein the at least one triggering signal ~~(26)~~ corresponds to a read operation.

12. (Currently Amended) The method according to claim 1, wherein the at least one triggering signal ~~(26)~~ corresponds to a write operation.

13. (Currently Amended) The method according to claim 1, wherein the at least one triggering signal ~~(26)~~ is a time clock pulse.

14. (Currently Amended) The method according to claim 1, wherein the at least one triggering signal ~~(26)~~ corresponds to the detection of a predetermined number of read/write operations or clock pulses.

15. (Currently Amended) The method according to claim 1, wherein said copying or relocating ~~(52, 52a)~~ of the data occurs a predetermined number of times between ~~the~~ triggering signals.

16. (Cancel)

17 (Currently Amended) The method according to claim 1, wherein all the data contained in the multi-block memory ~~(10)~~ is copied or relocated at the same time.

18. (Currently Amended) The method according to claim 1, further comprising the step of:

updating a variable logical address X after said copying or relocating in the multi-block memory ~~(10)~~ containing C memory elements, said variable logical address X for said C memory elements identified by pointers X_0, X_1 ...X_k, X_{k+1} ...X_{C-1} is updated to an updated variable logical address X_u for C-S memory elements identified by the pointers X_0, X_1 ...X_{k-1}, X_{k+S} ...X_{C-1}, wherein C is a total number of the memory elements of the multi-element memory ~~(10)~~, S is a number of the memory elements identified by the

pointers X_k, X_{k+1}, ... X_{k+S-1} in a spare memory block after said copying or relocating, wherein a first element of said first memory block ~~(17)~~ after said copying or relocating corresponds to a first element identified by the pointer X_k of the spare memory spare block after said copying or relocating.

19. (Currently Amended) The method according to claim 1 wherein at least one memory pointer pointing to said first memory block before said copying or relocating is updated to point to said second memory block after said copying or relocating.

20. (Currently Amended) An electronic device ~~(11)~~, comprising:

a multi-block memory ~~(10)~~ containing data, usable in multi-block memory ~~(10)~~ activities;

a memory wear controller ~~(22)~~, responsive to a triggering signal ~~(26)~~ or to a further triggering signal ~~(26a)~~, for providing a data-relocation signal ~~(30)~~ to the multi-block memory ~~(10)~~ to relocate the data from an at least one first memory block ~~(17)~~ containing an at least one memory element of the multi-block memory ~~(10)~~ to an at least one second memory block ~~(18)~~ of the multi-block memory ~~(10~~) wherein said at least one second memory block (18) does not contain said data before said copying or relocating, and for providing an update signal ~~(32)~~ after performing said copying or relocating; and

a memory pointer controller ~~(24)~~, responsive to the update signal ~~(32)~~,

wherein no information on a usage of said at least one first memory block, at least one second memory block or at least one memory element is provided for performing said copying or relocating..

21. (Currently Amended) The electronic device ~~(11)~~ of claim 20, wherein the memory pointer controller ~~(24)~~ provides a pointer signal ~~(34)~~ to the memory wear controller ~~(22)~~ based on predetermined criteria.

22. (Currently Amended) The electronic device ~~(11)~~ of claim 21, wherein the memory pointer signal ~~(34)~~ ~~contains~~ comprises a physical address Y ~~(Y)~~ in the multi-block memory ~~(10)~~ to be accessed for enabling an at least one further data relocation of the data located at the physical address Y ~~(Y)~~ and optionally further comprises an address of a first memory pointer M.

23. (Currently Amended) The electronic device ~~(11)~~ of claim 20, wherein the memory pointer controller ~~(24)~~ provides updating of at least one memory pointer pointing to said first memory block before said copying or relocating to point to said second memory block after said copying or relocating.

24. (Currently Amended) The electronic device ~~(11)~~ of claim 20, wherein the memory wear controller ~~(22)~~ and the memory pointer controller ~~(24)~~ are implemented as a combination of software and hardware components.

25. (Currently Amended) The electronic device ~~(11)~~ of claim 20, wherein the memory wear controller ~~(22)~~ and the memory pointer controller ~~(24)~~ are implemented as hardware.

26. (Currently Amended) The electronic device ~~(11)~~ of claim 25, wherein the hardware is implemented using a finite state machine ~~(15)~~.

27. (Currently Amended) The electronic device ~~(11)~~ of claim 20, wherein the memory wear controller ~~(22)~~ and the memory pointer controller ~~(24)~~ are implemented as software.

28. (Currently Amended) The ~~method~~ electronic device according to claim 20, wherein each of the at least one first memory block ~~(17)~~ and the at least one second memory block ~~(18)~~ contains only one memory element.

29. (Currently Amended) The electronic device ~~(11)~~ of claim 20, wherein there is more than one memory element contained in the at least one first memory block ~~(17)~~ and there is more than one memory element contained in the at least one second memory block ~~(18)~~, respectively.

30. (Currently Amended) The electronic device ~~(11)~~ of claim 20, wherein said copying or relocating of the data from the at least one first memory block ~~(17)~~ and updating the location of the memory pointers M, Z ~~(M, Z)~~ are performed according to predetermined criteria.

31. (Currently Amended) The electronic device ~~(11)~~ of claim 20, further comprising a triggering detector ~~(20)~~, responsive to the triggering signal ~~(26)~~, for providing a

further triggering signal ~~(26a)~~ upon detecting the triggering signal ~~(26)~~.

32. (Currently Amended) An electronic device, comprising:

means for containing data in multiple memory blocks, wherein said data is usable in activities of the means for containing data;

means for providing a data-relocation signal to the means for containing the data for copying or relocating the data from an at least one first memory block containing an at least one memory element of the means for containing the data to an at least one second memory block of the means for containing the data in response to a triggering signal, wherein said at least one second memory block does not contain said data before said copying or relocating, and for providing an update signal on a status of the means for containing the data after performing said copying or relocating; and

means for providing to the means for providing the data-relocation signal, in response to the update signal, a pointer signal ~~containing~~ comprising a physical address ~~pointer (Y)~~ Y in means for containing data to be accessed for enabling an at least one further data relocation of the data located at the physical address Y ~~(Y)~~ and optionally further comprising an address of a first memory pointer M ~~(M)~~,

wherein no information on a usage of said at least one first memory block, at least one second memory block or at least one memory element is provided for performing said copying or relocating.

33. (Currently Amended) The method according to ~~claim 1~~ claim 2, wherein the means for providing to the means providing the data-relocation signal further provides updating of at least one memory pointer pointing to said first memory block before said copying or relocating to point to said second memory block after said copying or relocating.

34. (Currently Amended) A method for wear leveling of a multi-block memory containing data, usable in multi-block memory activities, in which method said data is copied or relocated from an at least one first block containing an at least one memory element of the multi-block memory to an at least one second block containing an at least one memory element of the multi-block memory after detecting a triggering signal related to said data, wherein said at least one second block does not contain said data before said copying or relocating,

wherein no information on a usage of said at least one first memory block, at least one second memory block or at least one memory element is provided for performing said copying or relocating.

35. (Original) The method according to claim 34, wherein at least one memory pointer pointing to said first memory block before said copying or relocating is updated to point to said second memory block after said copying or relocating.